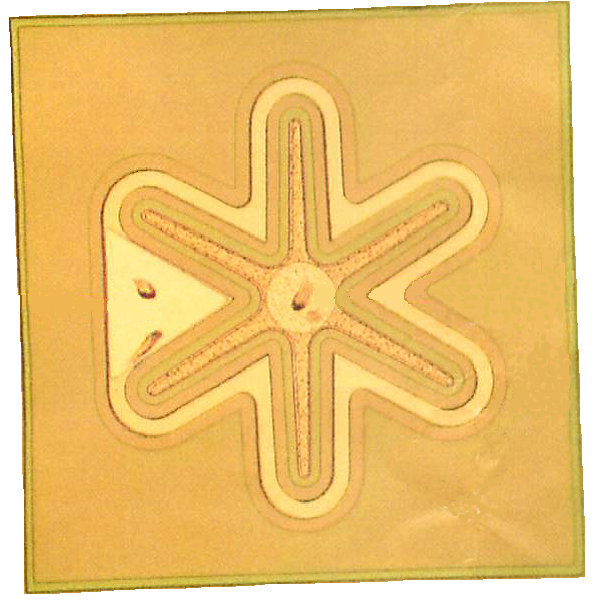
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**EMITTER**

**BASE**

**Top Material: Al**

**Backside Material: Au**

**Emitter: .004” X .004”**

**Base: .008” X .008”**

**Backside Potential: COLLECTOR**

**APPROVED BY: DK DIE SIZE .036” X .036” DATE: 10/4/21**

**MFG: MOTOROLA THICKNESS .006” P/N: 2N3499**

**DG 10.1.2**

#### Rev B, 7/19/02